IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please cancel claims 1-5, 7-11, and 13-22 without prejudice or disclaimer, amend claims 6 and 12, and add new claims 23-35 in accordance with the following:

1. (Cancelled).

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (currently amended) The logical equivalence verifying device according to claim ~~1~~23, wherein said display control section displays, based on the results of said logical equivalence verification, only those subcones for which said logical equivalence verification has resulted in mismatch.

7. (Cancelled)

8. (Cancelled)

9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (currently amended) The logical equivalence verifying device according to claim ~~1~~23, wherein said two prescribed circuits comprise a pre-change one and a post-change one of a circuit being designed when said circuit is changed.

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)

17. (Cancelled)

18. (Cancelled)

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Cancelled)

23. (New) A logical equivalence verifying device for performing logical equivalence verification of two prescribed circuits to display the results thereof, said device comprising:

a first identifier recording section that performs structural matching in which it is determined whether there are those portions in corresponding logic cones of said two circuits which correspond in circuit structure to each other, and records each result of said structural matching as an identifier for each element;

a subcone extracting section that extracts a plurality of collections of elements as subcones from each of said logic cones, each element collection including elements which are connected with each other and have the same identifier;

a verifying section that verifies logical equivalence between said two circuits for

each subcone extracted by said subcone extracting section; and

a display control section that displays a first group of subcones with mismatched results of said logical equivalence verification and a second group of subcones with matched results of said logical equivalence verification while distinguishing between these first and second groups of subcones based on the results of said logical equivalence verification,

wherein, when verification information on the subcone becomes mismatched, said display control section graphically displays the mismatched subcone.

24. (New) A logical equivalence verifying device for performing logical equivalence verification of two prescribed circuits to display the results thereof, said device comprising:

a first identifier recording section that performs structural matching in which it is determined whether there are those portions in corresponding logic cones of said two circuits which correspond in circuit structure to each other, and records each result of said structural matching as an identifier for each element;

a subcone extracting section that extracts a plurality of collections of elements as subcones from each of said logic cones, each element collection including elements which are connected with each other and have the same identifier;

a verifying section that verifies logical equivalence between said two circuits for each subcone extracted by said subcone extracting section; and

a display control section that displays a first group of subcones with mismatched results of said logical equivalence verification and a second group of subcones with matched results of said logical equivalence verification while distinguishing between these first and second groups of subcones based on the results of said logical equivalence verification,

wherein, said subcone extracting section extracts subcones in accordance with any one of the following manners (1) to (3):

(1) when the structures are matched to each other, said subcone extracting section extracting the structure as subcones;

(2) when instance names are matched to each other, said subcone extracting section extracting the instance names as subcones; and

(3) said subcone extracting section extracting subcones so that subcones in which an output point outputs a fixed value and the values of the output point become equal to one another are excluded.

25. (New) A logical equivalence verifying device for performing logical equivalence

verification of two prescribed circuits to display the results thereof, said device comprising:

a first identifier recording section that performs structural matching in which it is determined whether there are those portions in corresponding logic cones of said two circuits which correspond in circuit structure to each other, and records each result of said structural matching as an identifier for each element;

a subcone extracting section that extracts a plurality of collections of elements as subcones from each of said logic cones, each element collection including elements which are connected with each other and have the same identifier;

a verifying section that verifies logical equivalence between said two circuits for each subcone extracted by said subcone extracting section; and

a display control section that displays a first group of subcones with mismatched results of said logical equivalence verification and a second group of subcones with matched results of said logical equivalence verification while distinguishing between these first and second groups of subcones based on the results of said logical equivalence verification,

wherein, where a plurality of subcone mismatches are detected said verifying section verifies mismatch cause by assuming elements which exist in the mismatched subcones to be common mismatch cause candidates.

26. (New) The logical equivalence verifying device according to claim 24, wherein said display control section displays, based on the results of said logical equivalence verification, only those subcones for which said logical equivalence verification has resulted in mismatch.

27. (New) The logical equivalence verifying device according to claim 24, wherein said two prescribed circuits comprise a pre-change one and a post-change one of a circuit being designed when said circuit is changed.

28. (New) The logical equivalence verifying device according to claim 25, wherein said display control section displays, based on the results of said logical equivalence verification, only those subcones for which said logical equivalence verification has resulted in mismatch.

29. (New) The logical equivalence verifying device according to claim 25, wherein said two prescribed circuits comprise a pre-change one and a post-change one of a circuit being designed when said circuit is changed.

30. (New) A logical equivalence verifying method for performing logical equivalence verification of two prescribed circuits to display the results thereof, said method comprising:

performing structural matching in which it is determined whether there are those portions in corresponding logic cones of said two circuits which correspond in circuit structure to each other, and recording the results of said structural matching as an identifier for each element;

extracting a plurality of element collections as subcones from each of said logic cones, each element collection including elements which are connected with each other and have the same identifier;

performing logical equivalence verification between said two circuits for each of said subcones; and

displaying a first group of subcones with mismatched results of said logical equivalence verification and a second group of subcones with matched results of said logical equivalence verification while distinguishing between these first and second groups of subcones based on the results of said logical equivalence verification,

wherein, when verification information on the subcone becomes mismatched, said displaying graphically displays the mismatched subcone.

31. (New) A logical equivalence verifying method for performing logical equivalence verification of two prescribed circuits to display the results thereof, said method comprising:

performing structural matching in which it is determined whether there are those portions in corresponding logic cones of said two circuits which correspond in circuit structure to each other, and recording the results of said structural matching as an identifier for each element;

extracting a plurality of element collections as subcones from each of said logic cones, each element collection including elements which are connected with each other and have the same identifier;

performing logical equivalence verification between said two circuits for each of said subcones; and

displaying a first group of subcones with mismatched results of said logical equivalence verification and a second group of subcones with matched results of said logical equivalence verification while distinguishing between these first and second groups of subcones based on the results of said logical equivalence verification,

wherein, said extracting extracts subcones in accordance with any one of the

following manners (1) to (3):

(1) when the structures are matched to each other, extracting the structure as subcones;

(2) when instance names are matched to each other, extracting the instance names as subcones; and

(3) extracting subcones so that subcones in which an output point outputs a fixed value and the values of the output point become equal to one another are excluded.

32. (New) A logical equivalence verifying method for performing logical equivalence verification of two prescribed circuits to display the results thereof, said method comprising:

performing structural matching in which it is determined whether there are those portions in corresponding logic cones of said two circuits which correspond in circuit structure to each other, and recording the results of said structural matching as an identifier for each element;

extracting a plurality of element collections as subcones from each of said logic cones, each element collection including elements which are connected with each other and have the same identifier;

performing logical equivalence verification between said two circuits for each of said subcones; and

displaying a first group of subcones with mismatched results of said logical equivalence verification and a second group of subcones with matched results of said logical equivalence verification while distinguishing between these first and second groups of subcones based on the results of said logical equivalence verification,

wherein, where a plurality of subcone mismatches are detected said performing logical equivalence verification verifies mismatch cause by assuming elements which exist in the mismatched subcones to be common mismatch cause candidates.

33. (New) A computer-readable medium storing a program controlling a computer to execute a logical equivalence verifying method for performing logical equivalence verification of two prescribed circuits to display the results thereof, said method comprising:

performing structural matching in which it is determined whether there are those portions in corresponding logic cones of said two circuits which correspond in circuit structure to each other, and recording the results of said structural matching as an identifier for each element;

extracting a plurality of element collections as subcones from each of said logic cones, each element collection including elements which are connected with each other and have the same identifier;

performing logical equivalence verification between said two circuits for each of said subcones; and

displaying a first group of subcones with mismatched results of said logical equivalence verification and a second group of subcones with matched results of said logical equivalence verification while distinguishing between these first and second groups of subcones based on the results of said logical equivalence verification,

wherein, when verification information on the subcone becomes mismatched, said displaying graphically displays the mismatched subcone.

34. (New) A computer-readable medium storing a program controlling a computer to execute a logical equivalence verifying method for performing logical equivalence verification of two prescribed circuits to display the results thereof, said method comprising:

performing structural matching in which it is determined whether there are those portions in corresponding logic cones of said two circuits which correspond in circuit structure to each other, and recording the results of said structural matching as an identifier for each element;

extracting a plurality of element collections as subcones from each of said logic cones, each element collection including elements which are connected with each other and have the same identifier;

performing logical equivalence verification between said two circuits for each of said subcones; and

displaying a first group of subcones with mismatched results of said logical equivalence verification and a second group of subcones with matched results of said logical equivalence verification while distinguishing between these first and second groups of subcones based on the results of said logical equivalence verification,

wherein, said extracting extracts subcones in accordance with any one of the following manners (1) to (3):

(1) when the structures are matched to each other, extracting the structure as subcones;

(2) when instance names are matched to each other, extracting the instance names as subcones; and

(3) extracting subcones so that subcones in which an output point outputs a fixed value and the values of the output point become equal to one another are excluded.

35. (New) A computer-readable medium storing a program controlling a computer to execute a logical equivalence verifying method for performing logical equivalence verification of two prescribed circuits to display the results thereof, said method comprising:

performing structural matching in which it is determined whether there are those portions in corresponding logic cones of said two circuits which correspond in circuit structure to each other, and recording the results of said structural matching as an identifier for each element;

extracting a plurality of element collections as subcones from each of said logic cones, each element collection including elements which are connected with each other and have the same identifier;

performing logical equivalence verification between said two circuits for each of said subcones; and

displaying a first group of subcones with mismatched results of said logical equivalence verification and a second group of subcones with matched results of said logical equivalence verification while distinguishing between these first and second groups of subcones based on the results of said logical equivalence verification,

wherein, where a plurality of subcone mismatches are detected said performing logical equivalence verification verifies mismatch cause by assuming elements which exist in the mismatched subcones to be common mismatch cause candidates.